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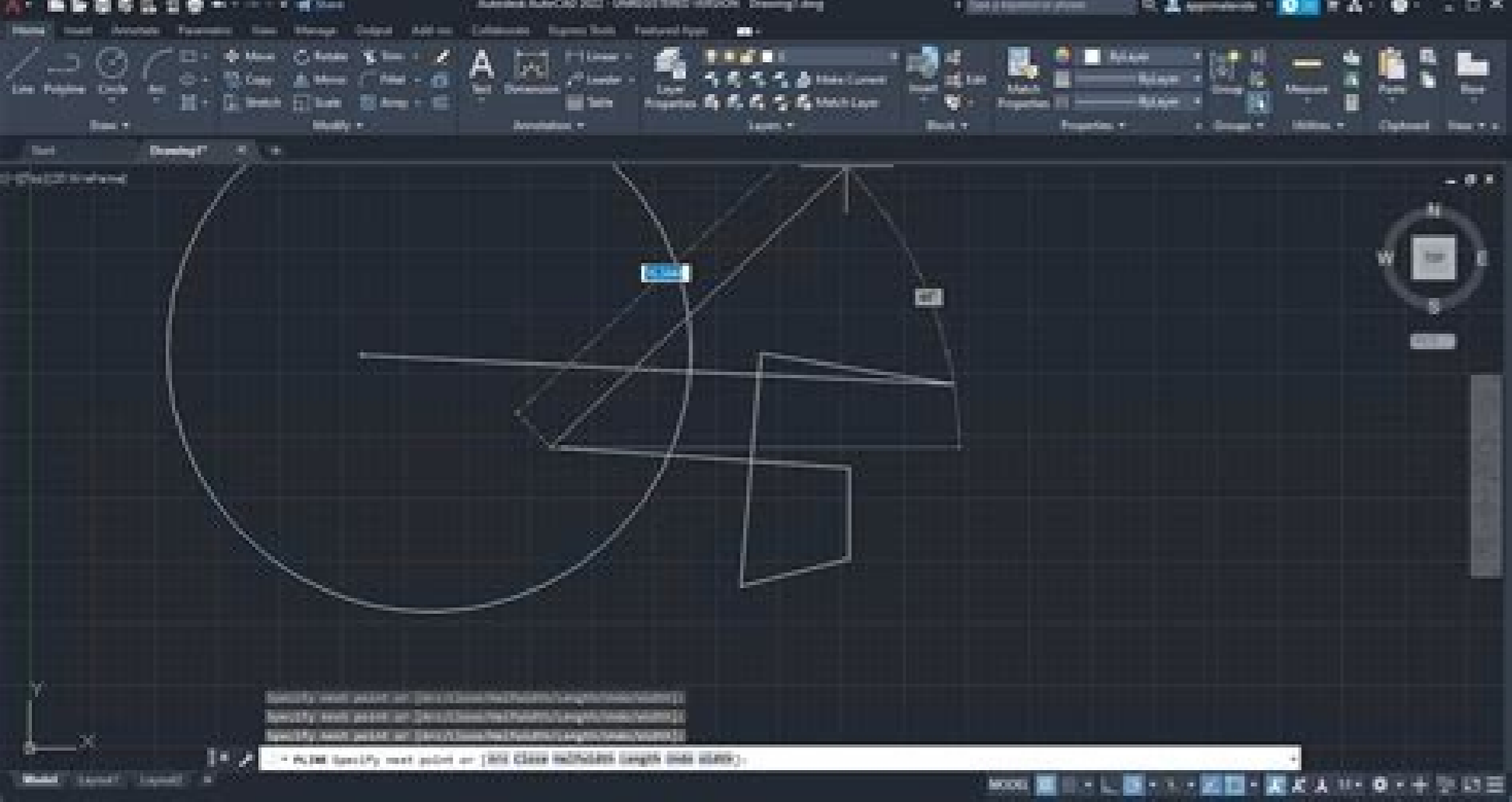
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With a real-time constraint-driven flow, you can easily set up your design rules and visually verify that your unique requirements are being met. This way you'll have less stress at signoff, reduce design respins, and improve time to market. High-speed and high-frequency designs contain critical signals that need to be managed early on. With real-time circuit analysis checks, you can identify and resolve any conflicts between signal lengths and complete your designs in a fraction of the time. Designs are vulnerable to SI and PI issues due to high data transfer rates, noise, improper component placement, and even poor power delivery networks (PDNs), to name a few. Poor SI and PI result in weak functionality and your design failing in the field. To avoid and ease these issues, it's important to simulate your design to identify and adjust those signals and planes that may be causing issues. Successfully bringing a product to market requires the efforts of several team members (whether they are working locally or remotely). Manually sharing design updates could cost you and your team time and productivity and increase the possibility of design errors. With a collaborative design environment, it's easy to avoid conflicting design data and get to market faster. A design reuse methodology means that not every project you work on must start from scratch. With existing and proven design IP, you can save time and prevent design errors. By reusing known-good modules and constraints, you can easily streamline your PCB design process and get to market with verified technology faster. Routing doesn't have to be a manual process filled with advanced routing techniques. With various routing modes and checks available, you can quickly complete complex routes on dense boards. Simply avoid rule violations and meet electrical, mechanical, spacing, and manufacturing requirements with the help of real-time visual cues. Packing complex technologies in a small area has its challenges, but with HDI technology and embedded components, it's possible to maintain SI and performance. Shorter signal paths and via stub elimination make it easy to create reliable, powerful, and compact designs. Real-time design for manufacturing (DFM) checks such as design for fabrication (DFF), design for assembly (DFA), and design for test (DFT) can help you identify potential problems while you design so you can avoid costly respins that could derail your project timeline. With these checks and detailed documentation, you can complete your design fast and sign off with confidence; That's design for excellence (DFX). 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It is designed for new customers who are evaluating or implementing a Cadence PCB flow or wanting to build a fully compatible library for use with the Allegro or OrCAD family of PCB design tools. A documented catalog of the Allegro/OrCAD Starter Library contents, as well as sample specifications used in the development of the library, is available in Adobe .pdf format. This "starter" or baseline library is provided free of charge for use with Allegro Design Entry HDL, OrCAD Capture, Allegro Design Entry CIS, and Allegro/OrCAD PCB Editor. It can be used "out of the box" or as a template from which customized parts can be created. The library is provided as a zipped archive, with installation and usage instructions included. Allegro PCB SI Cross-Section Library Extension The Cadence Allegro PCB SI Cross-Section Library Extension is a free download that extends the library of cross sections available on the release media. With this library extension, users of the 2D full-wave field solver will have access to increased numbers of pre-solved cross sections that will speed the time to solutions while using Allegro Signal Integrity (SI) products. This algorithm-based integrated model library (ABIML) provides solutions to cross sections using multiple-surface roughness algorithms and highly increases the likelihood of a match of cross sections in PCB and package designs that can be used by the Allegro SI tools to shorten the time to a full-wave 2D interconnect model that can be used in SI simulation. Allegro PCB SI cross Section Library Extension 16.3 - (388MB)

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